This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

Claims 1-2 (previously cancelled).

Claim 3 (currently amended): A row decoder for ~~applying a select voltage and a non-select voltage to select word lines and non-select word lines of a nonvolatile semiconductor storage device, the select word lines and the non-select word lines being determined according to an address signal, on a mode-by-mode basis for each of a program mode, a read mode and an erase mode~~ a nonvolatile semiconductor storage device, which comprises a plurality of blocks of floating gate field effect transistors arrayed along a column direction, wherein the floating gate field effect transistors respectively have a control gate, floating gate, a drain and a source and are electrically information programmable and erasable and wherein the floating gate field effect transistors are arrayed in a matrix shape on a substrate or well, and wherein the block comprises a plurality of row lines connected to the control gate of each of floating gate field effect transistor arrayed along a row direction, and a plurality of column lines connected via respective select transistors to the drain and source of each of floating gate field effect transistors arrayed along a column direction, and wherein the select transistors in each block are simultaneously turned on or off, the row decoder comprising:

control voltage output means for, on the mode-by-mode basis, outputting a control voltage responsive to select/non-select information which is determined according to the address signal;

select voltage output means for, on the mode-by-mode basis, outputting a select voltage responsive to a select state which is determined according to the address is signal;

non-select voltage output means for, on the mode-by-mode basis, outputting a non-select voltage responsive to a non-select state which is determined according to the address signal; and

applied voltage select means for, in the erase mode, selecting either one of the select voltage derived from the select voltage output means or the non-select voltage derived from the non-select voltage output means according to the control voltage derived from the control voltage output means, and simultaneously outputting the selected voltage to select word lines of one block while simultaneously outputting the non-selected voltage to non-select word lines of remaining blocks.

Claim 4 (currently amended): A row decoder for ~~applying a select voltage and a non-select voltage to select word lines and non-select word lines of a nonvolatile semiconductor storage device, the select word lines and the non-select word lines being determined according to an address signal, on a mode-by-mode basis for each of a program mode, a read mode and an erase mode~~ a nonvolatile semiconductor storage device, which comprises a plurality of blocks of floating gate field effect transistors arrayed along a column direction, wherein the floating gate field effect transistors respectively have a control gate, floating gate, a drain and a source and are electrically information programmable and erasable and wherein the floating gate field effect transistors are arrayed in a matrix shape on a substrate or well, and wherein the block comprises a plurality of row lines connected to the control gate of each of floating gate field effect transistor arrayed along a row direction, and a plurality of column lines connected via respective select transistors to the drain and source of each of floating gate field effect transistors arrayed

along a column direction, and wherein the select transistors in each block are simultaneously turned on or off, the row decoder comprising:

control voltage output means for, on the mode-by-mode basis, outputting a control voltage responsive to select/non-select information which is determined according to the address signal;

high voltage output means for, on the mode-by-mode basis, outputting a high voltage not less than a specified voltage responsive to a select state which is determined according to the address signal;

low voltage output means for, on the mode-by-mode basis, outputting a low voltage lower than the high voltage responsive to a non-select state which is determined according to the address signal; and

applied voltage select means for, in the erase mode, selecting either one of the high voltage derived from the high voltage output means or the low voltage derived from the low voltage output means according to the control voltage derived from the control voltage output means, and simultaneously outputting the high voltage to select word lines of one block as the select voltage while simultaneously outputting the low voltage to nonselect word lines of remaining blocks as the non-select voltage.

Claim 5 (currently amended): The row decoder according to Claim 3, wherein

in the erase mode, the select voltage is a positive voltage, while the non-select voltage is a negative voltage; and

an absolute value of the non-select voltage is equal to an absolute value of ~~the~~ a negative voltage applied to ~~the~~ a substrate or well of the nonvolatile semiconductor storage device.

Claim 6 (currently amended): The row decoder according to Claim 4, wherein

in the erase mode, the select voltage is a positive voltage, while the non-select voltage is a negative voltage; and

an absolute value of the non-select voltage is equal to an absolute value of ~~the~~ a negative voltage applied to ~~the~~ a substrate or well of the nonvolatile semiconductor storage device.